12 GHz Digital Frequency Synthesizer for FMCW Radar Applications

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Features

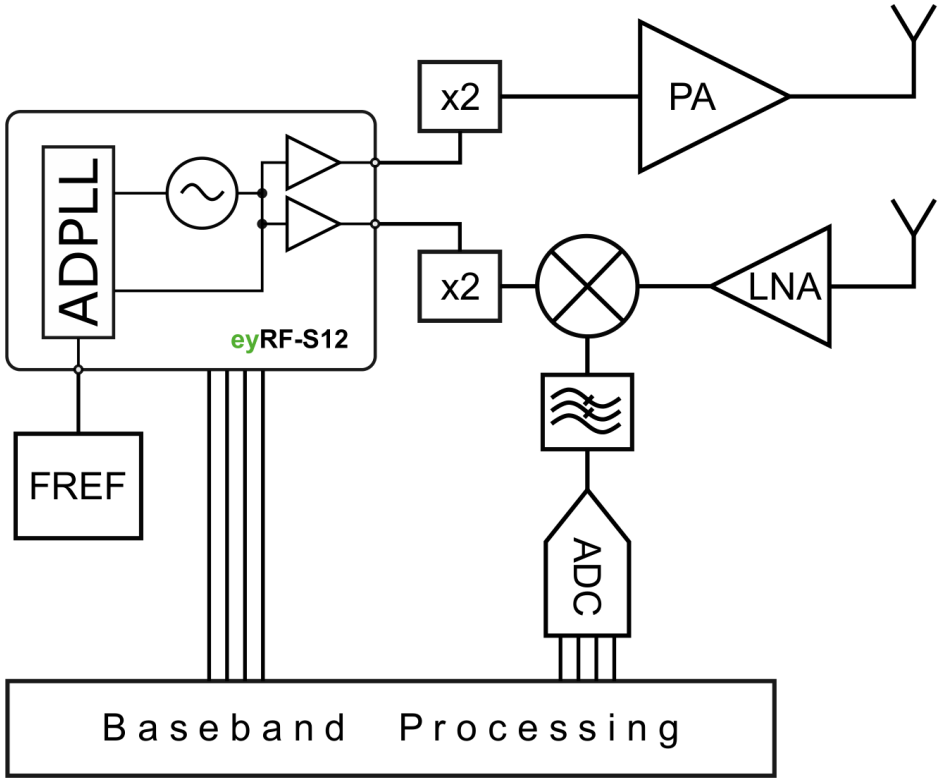
- Programmable Loop Filter
- FMCW Ramp Generation: 500MHz Bandwidth, 0.1ms-10ms Sweep Time
- FSK Modulator: 2MHz Bandwidth with 50 ksymb/s-100 ksymb/s
- Two-Point Modulation Scheme
- Calibration Algorithm for FMCW Ramp Linearization
- Integrated 12 GHz Oscillator
- Delay Measurement via integrated Time-to-Digital Converter

Application

- Near Field Radar Positioning
- Object Tracking
- Industrial Automation
- Industry 4.0

Description

eyRF-S12 is a fully integrated frequency synthesizer for FMCW radar applications. Since it is based on an all-digital Phase Locked Loop no external loop filter is necessary. Instead the loop bandwidth can be controlled and optimized via a digital interface. This, and the fact that oscillator and feedback loop are already implemented together in an integrated solution offers a time saving and area efficient possibility for the development of radar systems. The Time-to-Digital Converter (TDC) is adapted for the Digitally Controlled Oscillator (DCO) and offers very low closed loop phase noise. An integrated calibration algorithm enables highly linear and fast FMCW ramps.



AVDD=2.5V DVDD=1.2V, V_I/O=2.5V, REF=internal REF, TA=-40°C to 125°C

Parameter	Comment	Min	Typ	Max	Unit
REFERENCE CHARACTERISTICS					
FREF Input Frequency		50		150	MHz
FREF Input Capacitance				7	pF
Digitally Controlled Oscillator					
FREQUENCY CHARACTERISTIC					
Frequency Accuracy	Direct Tuning			100	kHz
	With Dithering			2	kHz
Number of Bits	Direct Tuning		18		Bits
	Dithering		6		Bits
	Calibration		5		Bits
Tuning Range		858		886	MHz
Frequency Range	With Calibration		1278		MHz
Minimum Frequency (Fmin)			11.905		GHz
Maximum Frequency (Fmax)			13.183		GHz
Output Power	At 50 Ohm Load	-2			dBm
NOISE CHARACTERISTIC					
Phase Noise at Fmin	@10 kHz Offset		-49.95		dBc/Hz
	@100 kHz Offset		-72.12		dBc/Hz
	@1 MHz Offset		-92.57		dBc/Hz
	@10 MHz Offset		-111.45		dBc/Hz
	@100 MHz Offset		-129.11		dBc/Hz
Phase Noise at Fmax	@10 kHz Offset		-51.58		dBc/Hz
	@100 kHz Offset		-82.65		dBc/Hz
	@1 MHz Offset		-98.63		dBc/Hz
	@10 MHz Offset		-123.20		dBc/Hz
	@100 MHz Offset		-143.55		dBc/Hz
DC CHARACTERISTICS					
Current Consumption	DCO Core		4.5		mA
Time-to-Digital Converter					
Resolution	Minimum Delay	20		25	ps
Number of Bits	TDC Output		64		Bits
	Fractional Phase Error		6		Bits
Loop Filter					
Programmable Loop Bandwidth	Configuration Range	$FREFx2^{-12}$		FREF	Hz
	Step Size m: Content of Register alpha		$FREFx2^{m-8}x2^{-4}$		Hz
Number of Bits	Scaling Coefficient Register: alpha		4		Bits
	Integration Coefficient Register: rho		4		Bits

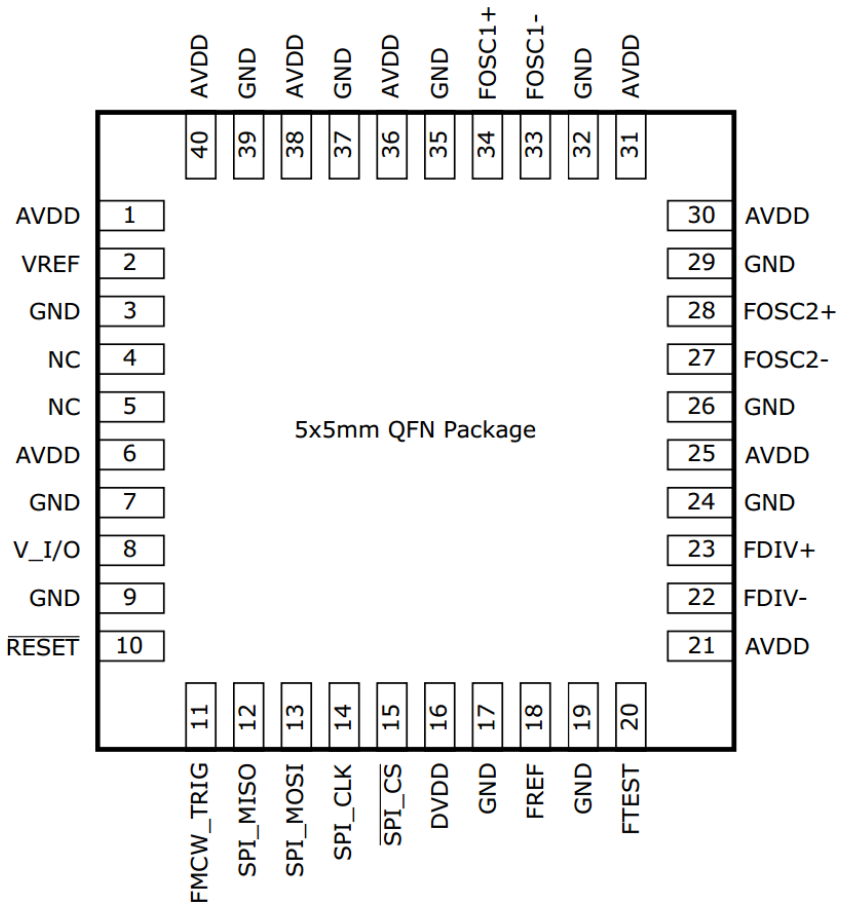
AVDD=2.5V DVDD=1.2V, V_I/O=2.5V, REF=internal REF, TA=-40°C to 125°C

Parameter	Comment	Min	Typ	Max	Unit
Modulator					
FSK					
Programmable Bandwidth	Configuration Range	1		8	MHz
Symbol rate	Configuration Range	50		100	ksymb/s
FMCW					
Programmable Bandwidth	Configuration Range			500	MHz
	Configuration Step Size				
Sweep Time		0.1		10	ms
Reference					
Initial Value	TA=25°C	1.14	1.2	1.26	V
Reference Drift			20		ppm/°C
Digital Interface					
DIGITAL INPUT		CMOS with Schmitt-Trigger			
V_{IL}		-0.3		0.3·IVDD	V
V_{IH}		0.7·V_I/O		V_I/O + 0.3	V
Input Capacitance			3		pF
Input Leakage Current		-1		1	uA
DIGITAL OUTPUTS					
V_{OL}	I_{load}=-100uA			0.3	V
V_{OH}		V_I/O - 0.3V		V_I/O	V
Load Capacitance			3		pF
Output Capacitance				30	pF
Power Consumption					
AVDD		2.25		2.75	V
DVDD		1.08		1.32	V
V_I/O		2.25		2.75	V
AIDD	Normal Operation			110	mA
	Power-Down		?		uA
IIDD+DIDD	Normal Operation			50	mA
	Power-Down		?		uA
Power Dissipation	Normal Operation			350	mW
	Power-Down		?		uW

Absolute maximum ratings

Parameter	Comment	Min	Typ	Max	Unit
Analog Supply Voltage	AVDD to GND	-0.3		2.8	V
FREF Input Voltage	FREF to GND	-0.3		AVDD + 0.3	V
Digital Supply Voltage	DVDD to GND	-0.3		1.44	V
Interface Supply Voltage	V_I/O to GND	-0.3		6	V
Interface Input Voltage		-0.3		IVDD + 0.3	V
Input currents to input pins		-10		10	mA
Ambient Temperature		-40		125	°C

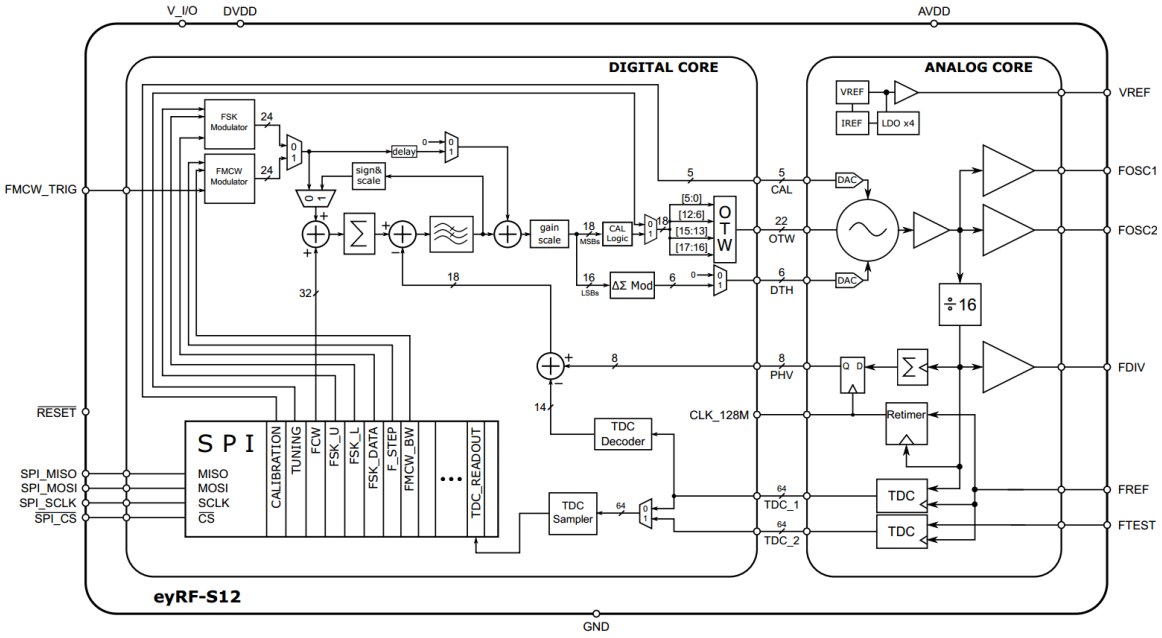
Pinout (5x5mm QFN package)



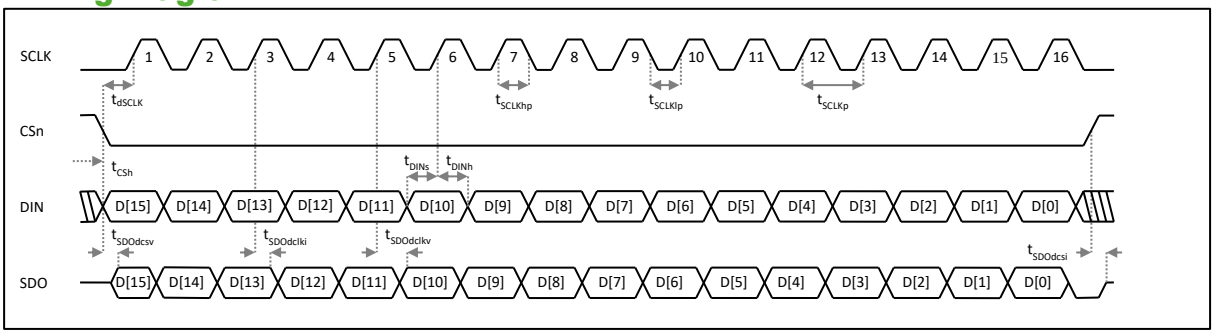
Pin Function Description

Pin			
No.	Name	TYPE	Pin Description
1	AVDD	P	2.5V Analog Supply Voltage
2	VREF	AO	Buffered Voltage Reference Output
3	GND	P	Ground
4	NC		Do not connect
5	NC		Do not connect
6	AVDD	P	2.5V Analog Supply Voltage
7	GND	P	Ground
8	V_I/O	P	2.5V Interface Supply Voltage
9	GND	P	Ground
10	$\overline{\text{RESET}}$	DI	Asynchronous Reset
11	FMCW_TRIG	DI	Trigger Input for enabling FMCW modulation
12	SPI_MISO	DO	SPI Communication: Master-Input-Slave Output
13	SPI_MOSI	DI	SPI Communication: Slave-Input-Master Output
14	SPI_CLK	DI	SPI Communication: Serial Clock
15	$\overline{\text{SPI\_CS}}$	DI	SPI Communication: Chip Select
16	DVDD	P	1.2V Digital Supply Voltage
17	GND	P	Ground
18	FREF	DI	Reference Frequency Input
19	GND	P	Ground
20	FTEST	DI	Input for TDC Testing (optional) – Connect to GND if not used
21	AVDD	P	2.5V Analog Supply Voltage
22	FDIV-	AO	Negative Divide-By-16 Output
23	FDIV+	AO	Positive Divide-By-16 Output
24	GND	P	Ground
25	AVDD	P	2.5V Analog Supply Voltage
26	GND	P	Ground
27	FOSC2-	AO	Secondary negative RF Output
28	FOSC2+	AO	Secondary positive RF Output
29	GND	P	Ground
30	AVDD	P	2.5V Analog Supply Voltage
31	AVDD	P	2.5V Analog Supply Voltage
32	GND	P	Ground
33	FOSC1-	AO	Primary negative RF Output
34	FOSC1+	AO	Primary positive RF Output
35	GND	P	Ground
36	AVDD	P	2.5V Analog Supply Voltage
37	GND	P	Ground
38	AVDD	P	2.5V Analog Supply Voltage
39	GND	P	Ground
40	AVDD	P	2.5V Analog Supply Voltage

Block Diagram



Timing Diagram



SPI data transfer

		MIN	MAX	Unit
t_{dSCLK}	Delay from falling CSn to first rising SCLK	TBD		ns
t_{SCLKhp}	High time of SCLK	5		ns
t_{SCLKlp}	Low time of CLK	5		ns
t_{SCLKp}	SCLK period	20		ns
f_{SCLK}	SCLK frequency		50	MHz
t_{CSh}	CSn high time	TBD		ns
t_{DINs}	Setup time of DIN after rising SCLK	TBD		ns
t_{DINh}	Hold time of DIN after rising CLK edge	TBD		ns
$t_{SDOdcsv}$	SDO valid after CSn falling		TBD	ns
$t_{SDOdclki}$	SDO invalid after rising SCLK	TBD		ns
$t_{SDOdclkv}$	DSDO valid after rising SCLK		TBD	ns
$t_{SDOdcsi}$	SDO in tristate after rising CS		TBD	ns

Overview

Based on an All-Digital Phase Locked Loop, eyRF-S12 generates a very stable frequency modulated signal in the range of 12 GHz to 12.5GHz which can be configured via an SPI interface. Fast and linear chirps are the groundwork for high precision positioning. The chirp duration is adjustable from 0.1ms to 10ms and the modulation frequency is programmable up to 500 MHz with 24 Bits resolution. An integrated software-controlled measurement of the oscillator's frequency characteristic triggers a linearization that makes highly linear frequency ramps possible. Phase noise and modulation speed can be optimized with the aid of two-point modulation and a programmable loop filter. Additionally, an FSK modulation enables the exchange of data between two radar stations.

Frequency Reference

The Chip has two inputs for the reference frequency. The signal frequency that should be used as the reference for the loop must be connected to the pin FREF. It should provide a square wave signal with a very stable frequency in the range of 50MHz to 150MHz to care for a good closed loop phase noise performance. The second input can be used for testing an additional Time-to-Digital Converter that is equivalent to the one used in the loop. Together with the signal connected to FREF it can be either used to optimize the TDC configuration by measuring its performance or use it to determine timing deviations of two clock signals.

Supplies

The internal circuitry operates from a 2.5V supply AVDD for analog components and 1.2V DVDD for the digital part. An additional 2.5V is used for I/O supply V_I/O. For an easy use, all supplies are internally stabilized with compensation capacitors larger than 1nF. This is true for AVDD to GND and DVDD to GND. Nevertheless, care should be taken that the decoupling capacitor is close to the supply pins. Wiring will add parasitic inductances, which together with parasitic capacitors could cause a chip-internal high frequency oscillation affecting the analog performance.

Frequency Modulation

The eyRF-S12 offers two modulation types. It can be configured to frequency shift keying (FSK) and FMCW mode to generate triangular frequency chirps. In FSK mode the data for communication is stored in the SPI register. A digital logic then shifts out bit after bit at a symbol rate of 50kHz-100kHz. A multiplexer then chooses one of two 8 Bit words FSK_U/L from SPI to tune the ADPLL to another frequency according to the FSK bandwidth. One of those is optional and can be set to zero permanently.

The FMCW Ramp is started via the external asynchronous signal connected to pin FMCW_TRIG. It then must be synchronized by the system clock CLK_128M. Since a new value of the ramp is calculated in each system clock cycle the sweep time is configured via the frequency step size FSTEP. By accumulating FSTEP and comparing it with a maximum value from the SPI register FMCW_BW that defines the FMCW bandwidth, a triangular chirp is achieved.

By enabling the two-point modulation scheme one can decouple the modulation speed from its loop bandwidth dependency. This feature enables a high flexibility, perfect for optimizing the performance of the synthesizer.

Time-to-Digital Converter

The TDC is used to measure the frequency deviation of the divided DCO output and the FREF input. Thus, it is one of the key components regarding the overall phase noise performance of the synthesizer. Based on delay lines the TDC is embedded in a Delay Locked Loop to enable a high and stable resolution which cares for a low noise synthesizer output frequency.

Loop Filter

The Filter consists of two paths. One multiplying the output of the phase detector and one optional integrating path that includes an accumulator after the scaling coefficient to configure the ADPLL as a type-II Loop. Both paths are added to form the filtered output. The type-I scaling coefficient is stored in the SPI Register as a 4 Bit two's complement value to realize left and right shifts of the phase error and thus perform multiplications in the type-I branch of the Filter. The integration coefficient is also configured via the SPI as a 4 Bit unsigned value to perform multiplications in the type-II branch of the Filter.

Serial Data Interface

The serial data input is configured via D[15] and D[14:10]. If D[15] is set to zero the Data Interface is in Read mode and the Bits D[14:0] are ignored. The Write mode is enable by setting D[15] to one. The input data D[9:0] then will be written into the register address specified by D[14:10].

Calibration Register (0x00)

CALIBRATION[7:0] – Data Input for the Digital-to-Analog Converter whose output tunes a small varactor that is connected in parallel to the LC Tank in the Digitally Controlled Oscillator. This data can be used to calibrate PVT variations and to ensure that the output frequency fully covers the desired frequency band

DCO_CAL – If this Bits is set to one the content of CALIBRATION[7:0] is shifted to the input of the coarse calibration DAC.

Tuning Register (0x01-0x02)

TUNING[17:0] – Data Input for direct Open Loop DCO tuning.

DCO_TUNE – If this Bit is set to one the content of TUNING[17:0] is shifted to the DCO.

FCW Register (0x03-0x06)

FCW[31:0] – The Frequency Command Word acts as the divider ratio between the Output and the Reference Frequency. The desired value can be calculated by the following formula.

$$FCW = \frac{F_{OUT}}{16 \cdot F_{REF}}$$

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	MSB	ADDRESS[4:0]					DATA[9:0]									
CALIBRATION	R/W	0	0	0	0	0	CALIBRATION[7:0]								-	DCO_CAL

Table 1: Calibration Register (DCO)

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	MSB	ADDRESS[4:0]					DATA[9:0]									
TUNING	R/W	0	0	0	0	1	TUNING[17:8]									
		0	0	0	1	0	TUNING[7:0]								-	DCO_TUNE

Table 2: Tuning Register

The 4 MSBs are Integer Bits. The residual 28 Bits are the fractional Part of the FCW. Thus, it covers a value range from 0 to $2^5 - 2^{-28}$.

FSK Register (0x06-0x09)

FSK_U[7:0] – This value adds to FCW and thus represents the upper frequency for FSK Modulation. It covers a value Range from 0 to $2^{-8} - 2^{-16}$.

FSK_L[7:0] - This value adds to FCW and thus represents the lower frequency for FSK Modulation. It covers a value Range from 0 to $2^{-8} - 2^{-16}$.

FSK_DATA[21:0] – Data to be sent by FSK.

FMCW_BW the upper limit for FMCW Modulation. It ranges from $0.5 - 2^{-25}$.

LOCK_DET (0x0E)

LOCK_THRESH[7:0] – Represents the threshold value for the Lock Detection Logic. Specifies how much the settled tuning word may vary over time to still be in lock. Values range from 0 to 15.9375 in steps of 0.0625.

LOCK – Switches between DCO direct tuning mode and ADPLL locked mode.

1: ADPLL is locked

0: Direct tuning mode

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	MSB	ADDRESS[4:0]					DATA[9:0]									
FCW	R/W	0	0	0	1	1	FCW[31:22]									
		0	0	1	0	0	FCW[21:12]									
		0	0	1	0	1	FCW[11:2]									

Table 3:Frequency Command Word Register

FSTEP (0x0A)

FSTEP[9:0] – Frequency step size for FMCW Modulation. In one Reference Clock cycle the Output Frequency will increase by this value. It adds to FCW and ranges from 0 to $2^{-15} - 2^{-25}$.

FMCW_BW (0x0B-0x0D)

FMCW_BW[23:0] – FSTEP is accumulated until it reaches FMCW_BW. Since FMCW_BW is added to FCW, FCW sets the lower limit and

SCALE (0x0F)

SCALE[7:0] – The output of the TDC has to be scaled to be limited between 0 and 1.

$$TDC_{out} = 1 - RISE \cdot SCALE$$

RISE is the decoded Time-to-Digital Converter output and nominally ranges from 0 to 64. SCALE ranges from 0 to $2^{-5} - 2^{-12}$. Thus, SCALE should be nominally set to 0x40.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	MSB	ADDRESS[4:0]					DATA[9:0]									
FCW/FSK	R/W	0	0	1	1	0	FCW[1:0]	FSK_U[7:0]								
FSK		0	0	1	1	1	FSK_L[7:0]									FSK_DATA[21:20]
		0	1	0	0	0	FSK_DATA[19:10]									
		0	1	0	0	1	FSK_DATA[9:0]									

Table 4:FCW/FSK Register

TDC_FIX – If this bit is set to 1 then the manual configuration of TDC resolution is enabled. The TDC resolution can then be trimmed by TDC_CTRL[1:0].

CONFIG (0x10)

TDC_TEST – Chooses the TDC whose output will be stored for read-out by the TDC Sampler.

0: TDC that is used in Feedback Loop

1: TDC with external input signals

TDC_SHIFT – On a rising edge of this Bit TDC Sampler writes Sampled TDC Output to TDC_DATA.

TDC_SAMPLE – enables TDC Output Sampling

TDC_MODE – If this bit is set to 1 then the manual configuration of TDC resolution is enabled. The TDC resolution can then be trimmed by TDC_CTRL[1:0].

TDC_CTRL[1:0] – Used for Trimming TDC resolution. Increasing TDC_CTRL decreases delay of one stage and thus increases TDC resolution.

MEAS – If this Bit is set to one the Loop is locked using the direct tuned DCO output frequency as reference. This way the data for Calibration Registers can be obtained.

CKD_EN – Enables output buffer for measuring divider output.

ENABLE – Global Chip Enable

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	MSB	ADDRESS[4:0]					DATA[9:0]									
FSTEP	R/W	0	1	0	1	0	FSTEP[9:0]									
FMCW_BW		0	1	0	1	1	FMCW_BW[23:14]									
		0	1	1	0	0	FMCW_BW[13:4]									
		0	1	1	0	1	FMCW_BW[3:0]				-	-	-	-	-	-

Table 5:FMCW Registers

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	MSB	ADDRESS[4:0]					DATA[9:0]									
LOCK_DET	R/W	0	1	1	1	0	LOCK_THRESH[7:0]								LOCK	-
SCALE		0	1	1	1	1	SCALE[7:0]								-	TDC_FIX

Table 6:Lock detection and Scale Register

MODE – Choose between FSK and FMCW Modulation.

0: FSK Modulation

1: FMCW Modulation

FILT (0x11)

DS_EN – Enables Delta Sigma DCO dithering.

TWO_PT_EN – Enables Two-Point Modulation.

A0[3:0] – Two's complement value to realize left and right shifts of Phase Error Information and thus perform multiplications from 2^{-8} to 2^{7} in the type I branch of the Filter.

B0[3:0] – Unsigned value to perform multiplications from 2^{-15} to 2^{0} in the type II branch of the Filter.

GAIN_SCALE (0x12)

K_DCO[7:0] – Scaling factor for Oscillator Tuning Word to adjust loop gain and compensate for DCO gain. This additional gain ranges from 0 to $2^{4} - 2^{-4}$.

TRIM (0x13)

CHPMP_TRIM[3:0] – Trim input for Charge Pump current in TDC Delay Locked Loop. Can be used to optimize DLL stability.

BG_TRIM[3:0] – Trimming input for the on Chip Bandgap reference voltage.

PD_BG – Power Down for TX Output

EDGE_CTRL – Enable Metastability protection for TDC (recommended to set to one).

CAL (0x14-0x16)

CAL_ADDR[5:0] – FMCW Ramp Calibration Register Address. Write calibration data in each of the 32 Registers to linearize FMCW Ramp.

CAL_R/W – Set this bit to one to write data stored in CAL_VAL[17:0] to Calibration Register with address CAL_ADDR[5:0].

CAL_EN – Enables FMCW Ramp Calibration.

CAL_VAL[17:0] – Calibration Data to be read/written from/to Calibration Register with

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	MSB	ADDRESS[4:0]					DATA[9:0]									
CONFIG	R/W	1	0	0	0	0	TDC_TEST	TDC_SHIFT	TDC_SAMPLE	TDC_MODE	TDC_CTRL[1:0]		MEAS	CKD_EN	ENABLE	MODE

Table 7:Configuration Register

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	MSB	ADDRESS[4:0]					DATA[9:0]									
FILT	R/W	1	0	0	0	1	DS_EN	TWO_PT_EN	A0[3:0]				B0[3:0]			
GAIN_SCALE		1	0	0	1	0	K_DCO[7:0]								-	-

Table 8: Filter/Loop Gain Settings

address CAL_ADDR[5:0].

TDC_DATA (0x17-0x1D)

TDC_DATA[63:0] – Data of one Sample of TDC Output. (Read-Only)

CAL_LOOP (0x1D-0x1F)

CAL_MEAS[17:0] – This register contains the averaged values of the Oscillator Tuning Word. (Read-Only)

SCALE_TDC (0x1F)

SCALE_CALC[6:0] – Read out the instantaneous ideal value for SCALE. (Read-Only)

LOCK_DET – If this bit can be read as one the loop is in lock. (Read-Only)

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	MSB	ADDRESS[4:0]					DATA[9:0]									
TRIM	R/W	1	0	0	1	1	CHPMP_TRIM[3:0]				BG_TRIM[3:0]				PD_BG	EDGE_CTRL
CAL		1	0	1	0	0	CAL_ADDR[5:0]						-	-	CAL_R/W	CAL_EN
		1	0	1	0	1	CAL_VAL[17:8]									
		1	0	1	1	0	CAL_VAL[7:0]								-	-

Table 10: Loop Calibration and Trim Registers

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	MSB	ADDRESS[4:0]					DATA[9:0]									
TDC_DATA	READ_ONLY	1	0	1	1	1	TDC_DATA[63:54]									
		1	1	0	0	0	TDC_DATA[53:44]									
		1	1	0	0	1	TDC_DATA[43:34]									
		1	1	0	1	0	TDC_DATA[33:24]									
		1	1	0	1	1	TDC_DATA[23:14]									
		1	1	1	0	0	TDC_DATA[13:4]									

Table 9: TDC Data Registers

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	MSB	ADDRESS[4:0]					DATA[9:0]									
TDC_DATA/CAL	READ_ONLY	1	1	1	0	1	TDC_DATA[3:0]				CAL_MEAS[17:12]					
CAL		1	1	1	1	0	CAL_MEAS[11:2]									
CAL/SCALE		1	1	1	1	1	CAL_MEAS[1:0]	SCALE_CALC[6:0]								LOCK_DET

Table 11: Read Only Loop Calibration Registers

Application

The eyRF-S12 is easy to use in the Application. There is no need to search for separate PLL and VCO ICs that fit in the application. Also, the design of an external Loop Filter to define an optimum, fixed loop bandwidth is not necessary. Instead, the digital approach offers a flexible solution in which the key parameters of the synthesizer can be reconfigured, adjusted and optimized without the need of hardware changes. That saves time and area in the implementation of the hardware for the application.